IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Economikos et al. Examiner: Vu, David

S/N. No.: 10/708,035 Group Art Unit: 2818

Filed.: February 4, 2006 Docket. No.: FIS920030391US1

Title: METHOD OF FORMING A TRENCH STRUCTURE

Honorable Commissioner for Patents P. O. Box 1450 Alexandria, VA 22313-1450

BRIEF OF APPELLANT

This Appeal Brief, pursuant to the Notice of Appeal filed April 6, 2007, is an appeal from the rejection of the Examiner in the Office Action dated January 8, 2007.

REAL PARTY IN INTEREST

International Business Machines, Inc. is the real party in interest.

RELATED APPEALS AND INTERFERENCES

None.

STATUS OF CLAIMS

Claims 1-10 are withdrawn. Claim 12 is canceled. Claims 11, and 13-24 are rejected. The rejection of claims 11 and 13-24 are being appealed.

STATUS OF AMENDMENTS

There are no After-Final Amendments, which have not been entered.

SUMMARY OF CLAIMED SUBJECT MATTER

A. CLAIM 11, INDEPENDENT

A method of fabricating a filled trench structure. The method comprises: (a) forming a planarization stop layer (110/120) on a top surface ((105) of a substrate (100); (b) forming a first set of trenches (135) in a first region (130) of said planarization stop layer (110/120) and said substrate (100) and forming a second set of trenches (145) in a second region (140) of said planarization stop layer (110/120) and said substrate (100), trenches in said first set of trenches (135) having a higher aspect ratio than said trenches (145) in said second region (140); (c) depositing a layer of a fill material (150) in and over said first and second sets of trenches (135/145) and on a top surface (125) of said planarization stop layer (110/120), said fill material (150) completely filling said trenches (135/145); (d) after step (c), removing, using a wet etching, a dry etching, a reactive ion etching or a plasma etching process, an uppermost layer of said fill material (150) from over said first and second sets of trenches (135/145) and said top surface (125) of said planarization stop layer (110/120), a thinned layer of said fill material (150) remaining over said first and second sets of trenches (135/145) and on said top surface (125) of said planarization stop layer (110/120), said fill material (150) still completely filling said first and second sets of trenches (135/145); and (e) after step (d), removing, using a planarization process, all said fill material (150) from said top surface (125) of said planarization stop layer (110/120) and over said first and second set of trenches (135/145), a top surface (160C) of said fill material (150) in said first set of trenches (135) and a top surface (160D) of said fill material

(150) in said second sets of trenches (145) co-planer with said top surface (125) of said planarization stop layer (110/120). See FIGs. 1, 2, 3, 5A, 5B, 6 and 7 and paragraphs [0015] to [0023] and [0030] to 0039].

B. CLAIM 22, INDEPENDENT

A method of fabricating a filled trench structure. The method comprises: (a) forming a planarization stop layer (110/120) on a top surface (105) of a substrate (100); (b) forming a first set of trenches (135) in a first region (130) of the planarization stop layer (110/120) and the substrate (100) and forming a second set of trenches (145) in a second region (140) of the planarization stop layer (110/120) and the substrate (100), trenches in the first set of trenches (145) having a higher aspect ratio than the trenches (145) in the second region (140); (c) depositing a layer of a fill material (150) in and over the first and second sets of trenches (135/145) and on a top surface (125) of the planarization stop layer (110/120), the fill material (150) completely filling the trenches (135/145); (d) after step (c), removing, using a nonplanarization process, an uppermost layer of the fill material (150) from over the first and second sets of trenches (135/145) and the top surface (125) of the planarization stop layer (110/120), a thinned layer of the fill material (150) remaining over the first and second sets of trenches (135/145) and on the top surface (125) of the planarization stop layer (110/120), the fill material (150) still completely filling the first and second sets of trenches (135/145); and (e) after step (d), removing, using a planarization process, all the fill material (150) from the top surface (125) of the planarization stop layer (110/120) and over the first and second set of trenches (135/145), a top surface (160C) of the fill material (150) in the first set of trenches (135) and a top surface (160D) of the fill material (150) in the second sets of trenches(145) co-planer with the top

surface (125) of the planarization stop layer (110/120). See FIGs. 1, 2, 3, 5A, 5B, 6 and 7 and paragraphs [0015] to [0023] and [0030] to 0039].

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

- 1. Claims 22-24 stand rejected under 35 U.S.C. 112, first paragraph, as allegedly failing to comply with the written description.
- 2. Claims 11, 13, 14 and 17-24 stand rejected under 35 U.S.C. §102(e) allegedly being anticipated by Jang et al. (US Pat. 6,869,858).
- 3. Claims 15, 16 and 20 stand rejected under 35 U.S.C. 103(a) as allegedly obvious over Jang et al. (US Pat. 6,869,858).

ARGUMENT

GROUND OF REJECTION 1

Claims 22-24 stand rejected under 35 U.S.C. 112, first paragraph, as allegedly failing to comply with the written description.

The Examiner rejected claims 22-24 under 35 U.S.C §112, (first paragraph) stating: "The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The original disclosure does not include teaching 'removing, using a non-planarization process...' (claim 22, step (d)). As shown in Appellants specification (fig. 4 and [0024], the step of removing a fill layer 150 is performed by a planarization process."

In response, Appellants note that paragraph [0024] and FIG. 4 do not describe the Appellants invention, but rather describe a problem of non-uniform planarization of fill layers discovered by Appellants that can occur when a planarization process (such as CMP) is used at this point (after the processes illustrated in FIGs 1, 2 and 3) in the simultaneous fabrication of different aspect ratio trenches. Appellants paragraph [0024] states "FIG. 4 is a partial cross-sectional view of semiconductor substrate 100 after a planarization process and illustrates non-uniform planarization of fill layer 150. In FIG. 4, a planarization process has been performed." Appellants paragraph [0025] describes what Appellants believe is the cause of the problem.

Appellants invention is a different process flow that solves the problem of non-uniform planarization of fill layers in the simultaneous fabrication of different aspect ratio trenches Appellants invention is illustrated in Appellants FIGs. 1, 2, 3, 5A, 5B, 6 and 7. Appellants

paragraph [0030] states: "FIGs. 5A and 5B are partial cross-sectional views of semiconductor substrate 100 illustrating preparation of the substrate according to a first embodiment of the present invention prior to planarization. In FIG. 5A a photoresist mask 165 is formed over fill layer 150 in second region 140. Photomask 165 may be formed by any of several methods well known in the art. In FIG. 5B, a wet etch is performed, reducing the size of and increasing the distance between the tops of hats 155 of FIG. 5A to the size and spacing of hats 155A of FIG. 5B." Appellants note that this supports "(d) after step (c), removing, using a non-planarization process, an uppermost layer of said fill material from over said first and second sets of trenches and said top surface of said planarization stop layer, a thinned layer of said fill material remaining over said first and second sets of trenches and on said top surface of said planarization stop layer, said fill material still completely filling said first and second sets of trenches" of Appellants claim 22. Appellants, therefore contend that the subject matter of claim 22 was clearly described in Appellants specification.

Appellants note claims 23 and 24 depend from claim 22 and no specific 35 U.S.C. 112 (first paragraph) rejection was given to claims 23 and 24.

Appellants request the 35 U.S.C. 112 (first paragraph) rejection of claims 22-24 be ordered withdrawn.

GROUND OF REJECTION 2

Claims 11, 13, 14 and 17-24 stand rejected under 35 U.S.C. §102(e) allegedly being anticipated by Jang et al. (US Pat. 6,869,858).

The Examiner rejected claim 11 (as well as claims 13, 14 and 17-24) under 35 U.S.C. §102(e) stating "Jang in figs. 6-11 disclose a method of fabricating a filled trench structure, comprising: forming a planarization stop layer 28 on a top surface of a substrate 10; forming a first set of trenches in a first region W2 of planarization stop layer and substrate and forming a second set of trenches in a second region W3 of planarization stop layer and substrate, trenches in first set of trenches having a higher aspect ratio than, trenches in second region (fig. 6 and col. 10, line 62 through col. 11, line 7); depositing a fill material 22 in first and second set of trenches and on a top surface of planarization stop layer 28, fill material completely filling trenches (col. 11, lines 8-28); removing an upper portion of fill material 22 by an etched back process (dry/wet etching) (fig. 7 and col. 11, lines 51-65); and (e) removing, using a planarization process, all fill material from top surface of planarization stop layer, a top surface of fill material in first and second sets of trenches co-planer with top surface of planarization stop layer (fig. 10)."

Appellants point out that Jang et al. describes two processes in FIGs. 6 through 11. The first process includes the steps illustrated in Jang et al. FIGs. 6, 7, 10 and 11 and the second includes the steps illustrated in Jang et al. FIGs. 6, 8, 9, 10 and 11, the difference being the substitution of the steps of FIGs. 9 and 10 for the step of FIG. 7.

First, Appellants contend that claim 11 is not anticipated by Jang et al. because Jang et al. does not teach each and every feature of claim 11. For example, Jang et al. does not teach "(d) after step (c), removing, using a non-planarization process, an uppermost layer of said fill

material from over said first and second sets of trenches and said top surface of said planarization stop layer, a thinned layer of said fill material remaining over said first and second sets of trenches and on said top surface of said planarization stop layer, said fill material still completely filling said first and second sets of trenches." Appellants respectfully point out that in FIG. 7 of Jang et al. fill layers 22a', 22b', 22c', and 22d' are not "completely filling the first and second trenches" as Appellants claim 11 requires. Appellants point out that top surfaces of fill layers 22a¹, 22b¹, 22c², and 22d² of Jang et al. FIG. 7 (and of FIG. 9 as well) are well below the top surface of the etch stop layers 28a, 28b, 28c and 28d (see Jang et al. FIG. 6). Further Jang et al. specifically teaches in col. 11, lines 55-59 referring to FIG. 7, "there has been etched back the blanket aperture fill layer 22 such that the thickness of the blanket aperture fill layer 22a', 22b', 22c', and 22d' within the apertures has been reduced to thickness less than the height of the mesa H." See Jang et al. FIG. 6 for "H" which includes the etch stop layer. The Examiner should also note that Appellants claim 11 defines the trenches to include that portion through the etch stop layer as well as the portion in the substrate, to wit: "(b) forming a first set of trenches in a first region of said planarization stop layer and said substrate and forming a second set of trenches in a second region of said planarization stop layer and said substrate."

Second, Appellants contend that the structure shown in Jang et al. FIG. 10 cannot be made from the structures shown in Jang et al. FIGs. 7 or 9. The Examiner indicated that FIG. 10 of Jang et al. taught "removing, using a planarization process, all fill material from top surface of planarization stop layer, a top surface of fill material in first and second sets of trenches coplaner with top surface of planarization stop layer (fig. 10)." Applicant point out that to get from Jang et al.FIG. 7 (or from Jang et al.FIG. 9) to Jang et al.FIG. 10 would require fills 22a', 22b', 22c', and 22d' to increase in thickness during the CMP process, which is impossible. While it is

possible to get to Jang et al. FIG. 10 from Jang et al.FIG. 8 directly, by skipping Jang et al.FIG. 9, this is taught as a CMP process and skips the wet etching steps of Jang et al. (see in col. 12, lines 48-56 of Jang et al., to wit "shown in FIG. 10...otherwise equivalent to the semiconductor integrated circuit...shown in FIG. 8 or FIG. 9 but where blanket fill dielectric layer 22a', 22b', 23c' and 22d'...have been chemical mechanical polish (CMP) planarized") which skips the requirement of Appellants claim 11, to wit "(d) after step (c), removing, using a wet-etching, a dry etching, a reactive etching or a plasma etching process, an uppermost layer of said fill material from over said first and second sets of trenches and said top surface of said planarization stop layer, a thinned layer of said fill material remaining over said first and second sets of trenches and on said top surface of said planarization stop layer."

Based on the preceding arguments, Appellants respectfully maintain that claim 11 is not unpatentable over Jang et al. and is in condition for allowance. Since claims 13-21 depend from claim 11, Appellants respectfully maintain that claims 13-21 are likewise in condition for allowance.

Appellants maintain the arguments presented *supra* with respect to claim 11 are applicable to claim 22 and that claim 22 is in condition for allowance. Appellants point out that Appellants claim 22 includes the limitation "(d) after step (c), removing, *using a non-planarization process*, an uppermost layer of said fill material from over said first and second sets of trenches and said top surface of said planarization stop layer, *a thinned layer of said fill material remaining over said first and second sets of trenches* and on said top surface of said planarization stop layer, said fill material still completely filling said first and second sets of trenches." Since claims 23 and 24 depend from claim 22, Appellants respectfully maintain that

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claims 23 and 24 are likewise in condition for allowance.

As to claim 14, Appellants contend that claim 14 is not anticipated by Jang et al. because Jang et al does not teach each and every feature of claim 14. For example, Jang et al. does not teach "between steps (c) and (d) forming a mask layer on said fill material in said second region, wherein in step (d) fill material is only removed from said first region." Appellants respectfully point out Jang et al., in FIG. 8 is removing fill material from the second region (22d") not the first region 22a, 22b, and 22c, the exact opposite of what Appellants are claiming. Compare Jang et al. FIG. 8 with Appellants FIG. 5A and 5B.

Based on the preceding arguments, Appellants respectfully maintain that claim 14 is not unpatentable over Jang et al. and is in condition for allowance.

As to claim 17, Appellants contend that claim 17 is not anticipated by Jang et al. because Jang et al does not teach each and every feature of claim 17. For example, Jang et al. does not teach "wherein said first region is a memory cell array region and said second region is a support circuit region of an integrated circuit." Appellants contend the Examiner has provided no evidence that Jang et al. teaches "wherein said first region is a memory cell array region and said second region is a support circuit region of an integrated circuit" as Appellants claim 17 requires.

Based on the preceding arguments, Appellants respectfully maintain that claim 17 is not unpatentable over Jang et al. and is in condition for allowance.

As to claim 19, Appellants contend that claim 19 is not anticipated by Jang et al. because Jang et al does not teach each and every feature of claim 19. For example, Jang et al. does not

teach "wherein the volume of fill material removed in step (d) is experimentally pre-determined to be a volume that allows removal in step (e) of all of said fill material from said top surface of said substrate in both said first and second regions in a predetermined amount of chemical-mechanical-polish or grind time." Appellants contend the Examiner has provided no evidence that Jang et al. teaches "wherein the volume of fill material removed in step (d) is experimentally pre-determined to be a volume that allows removal in step (e) of all of said fill material from said top surface of said substrate in both said first and second regions in a predetermined amount of chemical-mechanical-polish or grind time" as Appellants claim 19 requires.

Based on the preceding arguments, Appellants respectfully maintain that claim 19 is not unpatentable over Jang et al. and is in condition for allowance.

As to claim 20, Appellants contend that claim 20 is not anticipated by Jang et al. because Jang et al does not teach each and every feature of claim 20. For example, Jang et al. does not teach "wherein step (d) removes about 5 to 20% of the as deposited thickness of said fill material." Appellants contend the Examiner has provided no evidence that Jang et al. teaches "wherein step (d) removes about 5 to 20% of the as deposited thickness of said fill material." as Appellants claim 20 requires.

Based on the preceding arguments, Appellants respectfully maintain that claim 20 is not unpatentable over Jang et al. and is in condition for allowance.

As to claim 21, Appellants contend that claim 21 is not anticipated by Jang et al. because Jang et al does not teach each and every feature of claim 21. For example, Jang et al. does not teach "wherein step (d) reduces the *difference* between a volume of said fill material over first

region and a volume of said fill material over said second region.." Appellants contend the Examiner has provided no evidence that Jang et al. teaches "wherein step (d) reduces the difference between a volume of said fill material over first region and a volume of said fill material over said second region." as Appellants claim 21 requires.

Based on the preceding arguments, Appellants respectfully maintain that claim 21 is not unpatentable over Jang et al. and is in condition for allowance.

GROUND OF REJECTION 3

Claims 15, 16 and 20 stand rejected under 35 U.S.C. 103(a) as allegedly obvious over Jang et al. (US Pat. 6,869,858).

First, as to claim 15, 16 and 20, Appellants have argued *supra* in response to the Examiners § 102(e) rejection of claim 11 that claim 11 is allowable, since claims 15, 16 and 20 depends from claim 11, Appellants respectfully maintain that claims 15, 16 and 20 are not unpatentable over Jang et al. and are in condition for allowance.

Second, the Examiner rejected claims 15, 16 and 20 under 35 U.S.C §103 (a) stating that "Jang fails to disclose the fill material is removed about 5 to 20% of the as deposited thickness (claims 15&20); and the aspect ratio of the first/second trenches (claim 16). It would have been obvious to one with ordinary skill in the art at the time of the invention to perform an etched back process step as taught by Jang. The amount of the fill material being etched and the aspect ratio of the first/second trenches does not define patentable over Jang since it is well known processing variable and the discovery of the optimum or workable range involves only routine skill in the art. The specific amount of the semiconductor being etched does not provide any critical or unexpected results to the method of manufacturing a semiconductor device. Rather, it is merely an obvious selection of the etching amount based on desired functional characteristics determinable by routine experimentation. In Aller, the court stated, "Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller*, 220 F.2d 454, 456 105 USPQ 233,235 (CCPA 1995)."

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Appellants contend that the Examiner has offered no evidence that "the amount of fill material being etched" or the "aspect ratio" are processing variable effective to solve the problems described by Appellants in the simultaneous fabrication of different aspect ratio trenches known in the art. To the contrary, Appellants assert in paragraph [0025] to have discovered (i) the aspect ratio is not the primary cause of the problem and (ii) it is the volume of fill material that is the problem. Appellants state in paragraph [0025] that "the difference in removal rates of fill layer 150 is not a function of the values H1, H2, H3, and H4 as illustrated in FIG. 3, but of the relative volume of fill layer 150 in first and second regions 130 and 140." It is this discovery that forms the foundation for "removing about 5 to 20% of the as deposited thickness" that Appellants claim.

Based on the preceding arguments, Appellants respectfully maintain that claims 15, 16, and 20 are not unpatentable over Jang et al. and are in condition for allowance.

SUMMARY

In summary, Appellant respectfully requests reversal of the January 8, 2007 Office

Action rejection of claims 11 and 13-24.

Respectfully submitted,

FOR:

Dated: 06/01/2007

BY: Jack P. Friedman Reg. No. 44,688

FOR:

11.00

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APPENDIX A - CLAIMS ON APPEAL

11. A method of fabricating a filled trench structure, comprising:

(a) forming a planarization stop layer on a top surface of a substrate;

(b) forming a first set of trenches in a first region of said planarization stop layer and said

substrate and forming a second set of trenches in a second region of said planarization stop layer

and said substrate, trenches in said first set of trenches having a higher aspect ratio than said

trenches in said second region;

(c) depositing a layer of a fill material in and over said first and second sets of trenches

and on a top surface of said planarization stop layer, said fill material completely filling said

trenches;

(d) after step (c), removing, using a wet etching, a dry etching, a reactive ion etching or a

plasma etching process, an uppermost layer of said fill material from over said first and second

sets of trenches and said top surface of said planarization stop layer, a thinned layer of said fill

material remaining over said first and second sets of trenches and on said top surface of said

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planarization stop layer, said fill material still completely filling said first and second sets of trenches; and

- (e) after step (d), removing, using a planarization process, all said fill material from said top surface of said planarization stop layer and over said first and second set of trenches, a top surface of said fill material in said first set of trenches and a top surface of said fill material in said second sets of trenches co-planer with said top surface of said planarization stop layer.
- 13. The method of claim 11, wherein in step (e) said planarization process includes chemical-mechanical polishing or fixed abrasive grinding.
- 14. The method of claim 11, further including:

between steps (c) and (d) forming a mask layer on said fill material in said second region, wherein in step (d) fill material is only removed from said first region; and between steps (d) and (e) removing said masking layer.

- 15. The method of claim 14, wherein step (d) removes about 5 to 20% of an as deposited thickness of said fill material.
- 16. The method of claim 11, wherein the aspect ratio of trenches in said first set of trenches is greater than about 3:1 and the aspect ratio of trenches in said second region is less than about 3:1.
- 17. The method of claim 11, wherein said first region is a memory cell array region and said

second region is a support circuit region of an integrated circuit.

- 18. The method of claim 11, wherein said fill material is selected from the group consisting of: high-density plasma oxide, low-pressure chemical vapor deposition oxide, tetraethoxysilane oxide, silicon nitride, bis(tertiary-butylamine)silane, a thin layer of conformal insulator and a fill layer of N-doped, P-doped or un-doped polysilicon, tungsten, copper or aluminum.
- 19. The method of claim 11, wherein the volume of fill material removed in step (d) is experimentally pre-determined to be a volume that allows removal in step (e) of all of said fill material from said top surface of said substrate in both said first and second regions in a predetermined amount of chemical-mechanical-polish or grind time.
- 20. The method of claim 11, wherein step (d) removes about 5 to 20% of the as deposited thickness of said fill material.
- 21. The method of claim 11, wherein step (d) reduces the difference between a volume of said fill material over first region and a volume of said fill material over said second region.
- 22. A method of fabricating a filled trench structure, comprising:
 - (a) forming a planarization stop layer on a top surface of a substrate;
- (b) forming a first set of trenches in a first region of said planarization stop layer and said substrate and forming a second set of trenches in a second region of said planarization stop layer

and said substrate, trenches in said first set of trenches having a higher aspect ratio than said trenches in said second region;

- (c) depositing a layer of a fill material in and over said first and second sets of trenches and on a top surface of said planarization stop layer, said fill material completely filling said trenches;
- (d) after step (c), removing, using a non-planarization process, an uppermost layer of said fill material from over said first and second sets of trenches and said top surface of said planarization stop layer, a thinned layer of said fill material remaining over said first and second sets of trenches and on said top surface of said planarization stop layer, said fill material still completely filling said first and second sets of trenches; and
- (e) after step (d), removing, using a planarization process, all said fill material from said top surface of said planarization stop layer and over said first and second set of trenches, a top surface of said fill material in said first set of trenches and a top surface of said fill material in said second sets of trenches co-planer with said top surface of said planarization stop layer.
- 23. The method of claim 22, wherein in step (d) said non-planarization process includes a wet etching, a dry etching, a reactive ion etching or a plasma etching process.
- 24. The method of claim 22, wherein in step (e) said planarization process includes chemical-mechanical polishing or fixed abrasive grinding.

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APPENDIX B - EVIDENCE

There is no evidence entered by the Examiner and relied upon by Appellant in this appeal.

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APPENDIX C - RELATED PROCEEDINGS

There are no proceedings identified in the "Related Appeals and Interferences" section.